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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,348	12/04/2003	Todd Michael Burdine	ROC920030235USI	8616
30206	7590	05/18/2006	EXAMINER	
IBM CORPORATION ROCHESTER IP LAW DEPT. 917 3605 HIGHWAY 52 NORTH ROCHESTER, MN 55901-7829			BRITT, CYNTHIA H	
			ART UNIT	PAPER NUMBER
			2138	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/728,348	Applicant(s) BURDINE ET AL.	
	Examiner Cynthia Britt	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,3-8 and 10-18 is/are allowed.
- 6) ☐ Claim(s) ____ is/are rejected.
- 7) ☒ Claim(s) 2 and 9 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/4/03</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claims 1-18 are presented for examination

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 12/4/03 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Allowable Subject Matter

Claims 2 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forlenza et al. U.S Patent No. 6,308,290.

As per claims 1, 8, and 17, Forlenza et al. substantially teach the claimed circuit and method and program product in which generating scan chain diagnostic patterns prior to initial testing by using the SRSLs (registers that can be stimulated illustrated by the RSL ahead of the break of the FIGURES) and ORMLs (registers that can be observed illustrated by the registers after the break in the RMLs) in conjunction with system clocks and then applying these patterns conditionally to chips failing the flush

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and scan test. These patterns are generated in such a manner that they are independent of where the SR chain fails, but are then used to dynamically determine the failing SRL location for defective chips. The chips that cannot be diagnosed to a single latch are not considered for diagnostics or as potential PFA candidates. (Column 3 lines 33-44) Not disclosed by Forlenza is that the scan chain is coupled to an ABIST. However a person having ordinary skill in the art would have known that there are many testing arrangements and ABIST is merely a design choice and a specific type of BIST (column 6 lines 29-33).

As per claims 3 and 10, Forlenza et al. teach using the collected scan out data to identify the defective latch includes identifying a location of the defective latch in the scan chain (column 3 lines 61-63).

As per claims 4,5, and 11-12 Forlenza et al. teach performing at least one of a scan test and a flush test prior to applying the plurality of pattern sets to the scan chain, wherein applying the plurality of pattern sets includes laterally inserting each pattern set into the scan chain using the ABIST circuit (column 3 lines 9-31).

As per claims 6 and 13, Forlenza et al. teach collecting the scan out data includes serially stepping the scan out data through the scan chain to an output (column 4 lines 12-18).

As per claims 7 and 14, Forlenza et al. teach reconfiguring the scan chain prior to collecting the scan out data (column 4 lines 30-38).

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As per claims 15,16, and 18, the examiner would like to point out that storing the test code internally or externally or in what type of storage is merely a design choice based on applicant's intended use the prior art is replete with references showing various storage locations and types of storage for test code.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Gate Level Fault Diagnosis in Scan Based BIST" by Bayraktaroglu et al Proceedings of the 2002 Design automation and test in Europe Conference 1530-1591/02 IEEE

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Cynthia Britt
Examiner
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